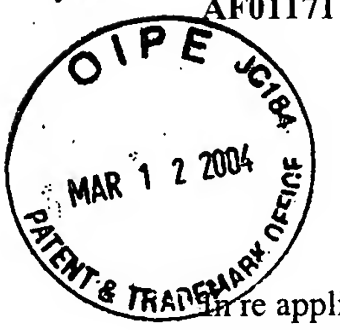
Image AF/2814

AF01171

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Angela Hui et al.

Serial No.:	10/032,757	Art Unit:	2814
Filed:	December 27, 2001	Examiner:	Marcos D. Pizarro Crespo

For: METHOD AND SYSTEM FOR FORMING DUAL GATE STRUCTURES IN A NONVOLATILE MEMORY USING A PROTECTIVE LAYER

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION - 37 CFR 1.192)

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on February 12, 2004.

NOTE: "The appellant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CFR 1.192(a) (emphasis added).

2. STATUS OF APPLICANT

This application is on behalf of

- ☒ other than a small entity
- ☐ small entity

verified statement:

- ☐ attached
- ☐ already filed

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☐	small entity	$165.00
☒	other than a small entity	$330.00
	Appeal Brief fee due	**$330.00**

CERTIFICATE OF MAILING (37 CFR § 1.8)

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: 3/8/04

Serena Beller
(Type or print name of person mailing paper)

Serena Beller
(Signature of person mailing paper)

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent applications. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply.

(complete (a) or (b) as applicable)

(a) ☐ Applicants petition for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

Extension (months)	Fee for other than small entity	Fee for small entity
☐ one month	$ 110.00	$ 55.00
☐ two months	$ 420.00	$ 210.00
☐ three months	$ 950.00	$ 475.00
☐ four months	$ 1,480.00	$ 740.00
Fee		

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

(b) ☒ Applicants believe that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicants have inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal Brief fee $330.00

Extension fee (if any) $0

TOTAL FEE DUE $330.00

6. FEE PAYMENT

☐ Attached is a check in the sum of $_____

☒ Charge Account No. 01-0365 (AF01171) the sum of $330.00.

A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

☒ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 01-0365 (AF01171).

AND/OR

☒ If any additional fee for claims is required, charge Account No. 01-0365 (AF01171).

Reg. No.: 47,159

SIGNATURE OF ATTORNEY

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184-P046US

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Angela Hui et al.
Serial No.:	10/032,757
Filed:	December 27,2001
Group Art Unit:	2814
Before the Examiner:	Marcos D. Pizarro Crespo
Title:	METHOD AND SYSTEM FOR FORMING DUAL GATE STRUCTURES IN A NONVOLATILE MEMORY USING A PROTECTIVE LAYER

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 8, 2004.

Serena Beller
Signature

Serena Beller
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 2-6 and 16-19 are pending. Claims 7-15 are withdrawn. Claims 2-6 and 16-19 stand rejected.

IV. STATUS OF AMENDMENTS

The Appellants' response to the Office Action, having a mailing date of February 25, 2003, has been considered, but the Examiner indicated that it did not place claims 2-6 and 16-19 in condition for allowance because Appellants' arguments were deemed unpersuasive.

V. SUMMARY OF INVENTION

Nonvolatile memory devices are used for a variety of applications. Specification, page 1, line 9. Such conventional semiconductor devices typically include a core and a periphery. Specification, page 1, lines 9-10. The core typically has a number of memory devices, each of which includes a core gate stack, a source at one end of the gate stack and a drain at the opposing end of the gate stack. Specification, page 1, lines 10-12. The core gate stack may include a polysilicon gate, a WSi layer, a polysilicon capping layer and a SiN or SiON layer. Specification, page 1, lines 13-14. Spacers may further be included at the ends of the gate stacks. Specification, page 1, lines 14-15. The periphery may include a plurality of devices where each device may include a conventional polysilicon gate and a WSi layer on the polysilicon gate. Specification, page 1, lines 15-17. A source and drain region

may be located at the opposing edges of the gate. Specification, page 1, lines 17-18. Spacers may further be included at the ends of the gate stacks. Specification, page 1, lines 19-20.

In order for such conventional semiconductor devices to function, electrical contract is made to the gate stacks at the core and the devices at the periphery. Specification, page 1, line 21 - page 2, line 1. Typically, electrical contact is made to the gate stacks at the core using the WSi layer. Specification, page 2, lines 1-2. Similarly, electrical contact is made to the gates at the periphery using the WSi layer. Specification, page 2, lines 2-3. Electrical contact to the sources and drains is also provided through a WSi layer. Specification, page 2, lines 3-4. As a result, electrical signals can be provided to the devices at the core and periphery of the conventional semiconductor device. Specification, page 2, lines 4-5.

The problems outlined above may at least in part be solved in some embodiments by including a CoSi layer above the polysilicon gate in the periphery gate stack. Specification, page 2, lines 19-21. In one embodiment of the present invention, a semiconductor device may comprise a plurality of core gate stacks in a core where each of the plurality of core gate stacks may include a first polysilicon gate and a WSi layer above the first polysilicon gate. Specification, page 2, lines 17-18. Further, each of the plurality of core gate stacks may include a polysilicon capping layer above the WSi layer an additional capping layer above the polysilicon capping layer. Specification, page 7, lines 1-6. The semiconductor device may further include a plurality of sources in the core where each of the plurality of sources resides between a portion of the plurality of core gate stacks. Specification, page 2, line 19. The semiconductor device may further include a plurality of periphery gate stacks in a periphery where each of the plurality of periphery gate stacks includes a second polysilicon gate and a CoSi layer above the second polysilicon gate. Specification, page 2, lines 19-21.

VI. ISSUES

A. Are claims 2-3 properly rejected under 35 U.S.C. §102(e) as being anticipated by Lien (U.S. Patent No. 6,338,993)?

B. Are claims 4-6 and 16-19 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Lien in view of Chang (U.S. Patent No. 5,981,339) and Yang (U.S. Patent No. 5,977,601)?

VII. GROUPING OF CLAIMS

Claims 2-3 form a first group.

Claims 4-6 and 16-19 form a second group.

The reasons for these groupings are set forth in Appellants' arguments in Section VIII.

VIII. ARGUMENT

A. Claims 2-3 are not properly rejected under 35 U.S.C. § 102(e) as being anticipated by Lien.

The Examiner has rejected claims 2-3 under 35 U.S.C. §102(e) as being anticipated by Lien. Paper No. 8, pages 2-3. Appellants respectfully traverse these rejections for at least the reasons stated below.

For a claim to be anticipated over 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference. M.P.E.P. §2131.

Appellants respectfully assert that Lien does not disclose "a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality of core gate stacks" as recited in claim 2. The Examiner cites element 400 in Figure 7 of Lien as disclosing the above-cited claim limitation. Paper No. 8, pages 3 and 6. Appellants respectfully traverse and assert that Lien instead discloses depositing a silicon nitride layer 400 over the memory cell region 30, the NMOS region 20 and the

PMOS region 10 and atop the gate structures on these regions. Column 3, lines 56-59. Lien further discloses that the silicon nitride layer 400 is used as a protective layer of the memory cell region 30 in a salicide process. Column 3, lines 59-61. Lien further discloses that the silicon nitride layer 400 is etched to form silicon nitride spacers 420 of the gate structure on the NMOS region. Column 4, lines 2-4. Hence, Lien discloses etching the silicon nitride layer to form spacers in the peripheral logic region. However, Lien does not disclose that the silicon nitride layer 400 in the memory cell region is etched to form spacers. Instead, Lien discloses that the memory cell region is protected by the silicon nitride layer 400 as illustrated in Figure 7. Thus, Lien does not disclose all of the limitations of claim 2, and thus Lien does not anticipate claim 2. M.P.E.P. §2131.

As a result of the foregoing, Appellants respectfully assert that not each and every claim limitation was found within Lien and thus claims 2-3 are not anticipated by Lien.

B. Claims 4-6 and 16-19 are not properly rejected under 35 U.S.C. §103(a) as being unpatentable over Lien in view of Chang and Yang.

The Examiner has rejected claims 4-6 and 16-19 under 35 U.S.C. §103(a) as being unpatentable over Lien in view of Chang and Yang. Paper No. 8, page 4. Appellants respectfully traverse these rejections for at least the reasons stated below.

1. The Examiner has not provided any objective evidence for combining Lien with either Chang or Yang.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q. 2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q. 2d 1313, 1317 (Fed. Cir.

2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Lien with Chang to have a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon, as recited in claim 4 and similarly in claim 16, is "to prevent cracking of the silicide layer." Paper No. 8, page 5. Further, the Examiner's motivation for modifying Lien with Yang to have a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon, as recited in claim 4 and similarly in claim 16, is "to improve the density of the core of gate stacks." Paper No. 6, page 5. These motivations are insufficient to support a *prima facie* case of obviousness since they are merely the Examiner's subjective opinion.

Lien teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process. Column 2, lines 8-22.

Chang, on the other hand, teaches a method for forming a flash memory cell which permit efficient erasure operations while minimizing problems (e.g., "smiling face" phenomenon, small number of large oxide valley formations under the floating gate) associated with conventional flash memory cells and conventional fabrication techniques. Column 2, line 45 – Column 3, line 19.

Yang, on the other hand, teaches a memory gate stack that has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV) lithography techniques by depositing a layer of silicon oxynitride over a plurality of layers and a thin resist layer overlying on the silicon oxynitride layer. Abstract.

The Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining a reference (Lien) that teaches performing

a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process with a reference (Chang) that teaches a method for forming a flash memory cell which permit efficient erasure operations while minimizing problems (e.g., "smiling face" phenomenon., small number of large oxide valley formations under the floating gate) associated with conventional flash memory cells and conventional fabrication techniques. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). There is no suggestion in Lien of solving problems associated with erase operations. Neither is there any suggestion in Lien of solving the "smiling face" phenomenon. Neither is there any suggestion in Lien of solving the problem of oxide valley formations. Since the Examiner has not submitted objective evidence for modifying Lien with Chang, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining a reference (Lien) that teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process with a reference (Yang) that teaches a memory gate stack that has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV) lithography techniques by depositing a layer of silicon oxynitride over a plurality of layers and a thin resist layer overlying on the silicon oxynitride layer. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). There is no suggestion in Lien of having a memory gate stack that has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV) lithography techniques. Neither is there any suggestion in Lien of having a memory gate stack that has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV) lithography techniques by depositing a layer of silicon oxynitride over a plurality of layers and a thin resist layer overlying on the silicon oxynitride

layer. Since the Examiner has not submitted objective evidence for modifying Lien with Yang, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Lien to have a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). There is no suggestion in Lien of having a polysilicon layer above the WSi layer and a capping layer above the polysilicon layer. Since the Examiner has not submitted objective evidence for modifying Lien to have a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *Id.*

Furthermore, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Lien to prevent cracking of the silicide layer (Examiner's motivation). *Id.* The Examiner's motivation appears to have been gleaned from the secondary reference (Chang). The Examiner has cited to column 6, lines 1-2 of the secondary reference (Chang) as support for the Examiner's motivation. Paper No. 8, page 4. This is not evidence as to why one of ordinary skill in the art with the primary reference (Lien) in front of him would have modified the primary reference (Lien) with a secondary reference (Chang). The primary reference (Lien) teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process. The Examiner must provide evidence as to why one of ordinary skill in the art with the primary reference (Lien) in front of him, which teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process, would be modified with a secondary reference (Chang)

which teaches a method for forming a flash memory cell which permit efficient erasure operations while minimizing problems (e.g., "smiling face" phenomenon., small number of large oxide valley formations under the floating gate) associated with conventional flash memory cells and conventional fabrication techniques. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000) Merely stating what the secondary reference teaches is not evidence for combining a primary reference (Lien) with the secondary reference (Chang). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

Furthermore, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Lien to improve the density of the core of gate stacks (Examiner's motivation). *Id.* The Examiner's motivation appears to have been gleaned from the secondary reference (Yang). The Examiner has cited to column 4, lines 23-26 and column 5, lines 39-46 of the secondary reference (Yang) as support for the Examiner's motivation. Paper No. 8, page 5. This is not evidence as to why one of ordinary skill in the art with the primary reference (Lien) in front of him would have modified the primary reference (Lien) with a secondary reference (Yang). The primary reference (Lien) teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process. The Examiner must provide evidence as to why one of ordinary skill in the art with the primary reference (Lien) in front of him, which teaches performing a salicide process to form a salicide layer on the source/drain regions of the logic cell region where the gate structure of the memory cell region is protected by the silicon nitride layer during the salicide process, would be modified with a secondary reference (Yang) which teaches a memory gate stack that has spaces on the order of less than 0.25 microns using conventional deep ultraviolet (DUV)

lithography techniques by depositing a layer of silicon oxynitride over a plurality of layers and a thin resist layer overlying on the silicon oxynitride layer. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1433-1434 (Fed. Cir. 2002); *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1318 (Fed. Cir. 2000) Merely stating what the secondary reference teaches is not evidence for combining a primary reference (Lien) with the secondary reference (Yang). *See Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002).

2. By combining Lien with Chang, the principle of operation of Lien would change.

If the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactorily for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellants submit that by combining Lien with Chang, the principle of operation in Lien would change and subsequently render the operation of Lien to perform its purpose unsatisfactorily.

Lien teaches a doped polysilicon gate formed on a gate oxide layer of the memory cell region and a tungsten silicide layer formed on the doped polysilicon gate. Column 3, lines 43-45. Lien further teaches a cap layer (e.g., TEOS material or silicon nitride) formed on the tungsten silicide layer. Column 3, lines 45-46. Lien further teaches that the memory cells of the embedded DRAM are protected by a silicon nitride layer (over the cap layer) during the salicide process of the logic cells in the device. Column 3, lines 56-63.

Chang, on the other hand, teaches that a phosphorous doped amorphous polysilicon layer is deposited via LPCVD to form an in situ phosphorous doped polysilicon layer 48. Column 5, lines 51-43. Chang further teaches a poly-cap layer 52 deposited over the tungsten silicide layer 50. Column 5, lines 65-55. Chang further teaches that a capping layer 54, for example, of SiON is deposited over the poly-cap layer 52. Column 6, lines 2-4. Chang does not teach depositing a silicon nitride layer over capping layer 54 to protect a memory cell region.

Hence, by combining Lien and Chang, Lien would not be able to form the gate structure of the memory cells consisting of the layers of a doped polysilicon gate, a tungsten silicide layer formed on the doped polysilicon gate, and a cap layer formed on the tungsten silicide layer. Instead, Lien would have to be modified to have the gate structure of the memory cells include the layers of a capping layer overlying a poly-cap layer overlying a tungsten silicide layer overlying a phosphorous doped polysilicon layer. Further, Lien would no longer have a silicon nitride layer deposited over the memory cell region, including the capping layer, as Chang does not teach depositing a silicon nitride layer over capping layer 54 to protect a memory cell region. Hence, by modifying Lien to include the layers of the memory cell region of Chang, Lien would not be able to protect the gate structure of the memory cell region by the silicon nitride layer during the salicide process since the silicon nitride layer would not exist. Hence, by combining Lien with Chang, the principle of operation in Lien would change and subsequently render the operation of Lien to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

3. By combining Lien with Yang, the principle of operation of Lien would change.

If the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactorily for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Appellants submit that by combining Lien with Yang, the principle of operation in Lien would change and subsequently render the operation of Lien to perform its purpose unsatisfactorily.

As stated above, Lien teaches a doped polysilicon gate formed on a gate oxide layer of the memory cell region and a tungsten silicide layer formed on the doped polysilicon gate. Column 3, lines 43-45. Lien further teaches a cap layer formed on the tungsten silicide layer. Column 3, lines 45-46. Lien further teaches that the memory cells of the embedded DRAM are protected by a silicon nitride layer during the salicide process of the logic cells in the device. Column 3, lines 56-63.

Yang, on the other hand, teaches a plurality of layers formed overlying the substrate where the plurality of layers include a first polysilicon layer 62 and an oxide-nitride-oxide (ONO) layer 64 overlying on the first polysilicon layer 62. Column 4, lines 13-18. Yang further teaches that the plurality of layers further includes a second polysilicon layer 66 overlying on the ONO layer 64. Column 4, lines 19-20. Yang further teaches that the plurality of layers further includes a silicide layer 68 overlying on the second polysilicon layer 66. Column 4, lines 20-22. Yang further teaches that the plurality of layers further includes a polysilicon cap layer 70 overlying on the silicide layer 68. Column 4, lines 22-23. Yang further teaches that the plurality of layers further includes the silicon oxynitride(SiON) layer 72 overlying

on the polysilicon cap layer 70. Column 4, lines 23-24. Yang does not teach depositing a silicon nitride layer over layer 72 to protect a memory cell region.

Hence, by combining Lien and Yang, Lien would not be able to form the gate structure of the memory cells consisting of the layers of a doped polysilicon gate, a tungsten silicide layer formed on the doped polysilicon gate, and a cap layer formed on the tungsten silicide layer. Instead, Lien would have to be modified to have the gate structure of the memory cells include the layers of a silicon oxynitride layer overlying a polysilicon layer overlying a silicide layer overlying a second polysilicon layer overlying an ONO layer overlying a first polysilicon layer. Further, Lien would no longer have a silicon nitride layer deposited over the memory cell region, including the capping layer (silicon oxynitride layer), as Yang does not teach depositing a silicon nitride layer over layer 72 (silicon oxynitride layer) to protect a memory cell region. Hence, by modifying Lien to include the layers of the memory cell region of Yang, Lien would not be able to protect the gate structure of the memory cell region by the silicon nitride layer during the salicide process since the silicon nitride layer would not exist. Hence, by combining Lien with Yang, the principle of operation in Lien would change and subsequently render the operation of Lien to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 4-6 and 16-19. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

IX. CONCLUSION

For the reasons noted above, the rejections of claims 2-6 and 16-19 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 2-6 and 16-19.

Respectfully submitted,
WINSTEAD SECHREST & MINICK P.C.
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APPENDIX

2 A semiconductor device including a core and a periphery, the semiconductor device comprising:

a plurality of core gate stacks in the core, each of the plurality of core gate stacks including a first polysilicon gate and a WSi layer above the first polysilicon gate, wherein each of the plurality of core gate stacks includes an edge;

a plurality of core spacers, each of the plurality of core spacers residing along an edge of the plurality core gate stacks;

a plurality of sources in the core, the plurality of sources residing between a portion of the plurality of core gate stacks; and

a plurality of periphery gate stacks in the periphery, each of the plurality of periphery gate stacks including a second polysilicon gate and a CoSi layer on the second polysilicon gate.

3. The semiconductor device of claim 2 wherein each of the plurality of periphery gate stacks includes an edge, the semiconductor device further comprising:

a plurality of periphery spacers, each of the plurality of periphery spacers residing along an edge of the plurality periphery gate stacks.

4. The semiconductor device of claim 2 wherein each of the plurality of core gate stacks includes the first polysilicon gate, the WSi layer above the first polysilicon gate, a layer of polysilicon above the WSi layer and a capping layer above the layer of polysilicon.

5. The semiconductor device of claim 4 wherein the capping layer is a SiN layer.

6. The semiconductor device of claim 4 wherein the capping layer is a SiON layer.

16. A semiconductor device comprising:

a plurality of core gate stacks in a core, wherein each of said plurality of core gate stacks comprises a first polysilicon gate and a WSi layer above said first polysilicon gate and a polysilicon capping layer above said WSi layer and an additional capping layer above said polysilicon capping layer;

a plurality of sources in said core, wherein said plurality of sources resides between a portion of said plurality of core gate stacks; and

a plurality of periphery gate stacks in a periphery, wherein each of said plurality of periphery gate stacks comprises a second polysilicon gate and a CoSi layer above said second polysilicon gate.

17. The semiconductor device as recited in claim 16, wherein said additional capping layer functions as an antireflective layer.

18. The semiconductor device as recited in claim 16, wherein said additional capping layer is a SiN layer.

19. The semiconductor device as recited in claim 16, wherein said additional capping layer is a SiON layer.